

ABSTRACT OF THE DISCLOSURE

In one embodiment of the present invention, a slave interface circuit includes a slave access circuit and a slave bus decoder. The slave access circuit provides access to the one of P slave devices from one of N master processors via a system bus controller and K slave buses. The K slave buses are configured to couple to the P slave devices. The system bus controller dynamically maps address spaces of the P slave devices. The slave bus decoder enables the one of the P slave devices to connect to one of the K slave buses when the one of the P slave devices is addressed by the one of the N master processors. The slave bus decoder is controlled by the system bus controller. In another embodiment of the present invention, the system bus controller includes an arbiter, a mapping circuit, and a switching circuit. The arbiter arbitrates access requests from N master processors via N master buses and generates arbitration signals. The mapping circuit stores mapping information to dynamically map an address space of K slave devices coupled to K slave buses based on the arbitration signals. The switching circuit connects the N master buses to K slave buses based on the arbitration signals and the mapping information.